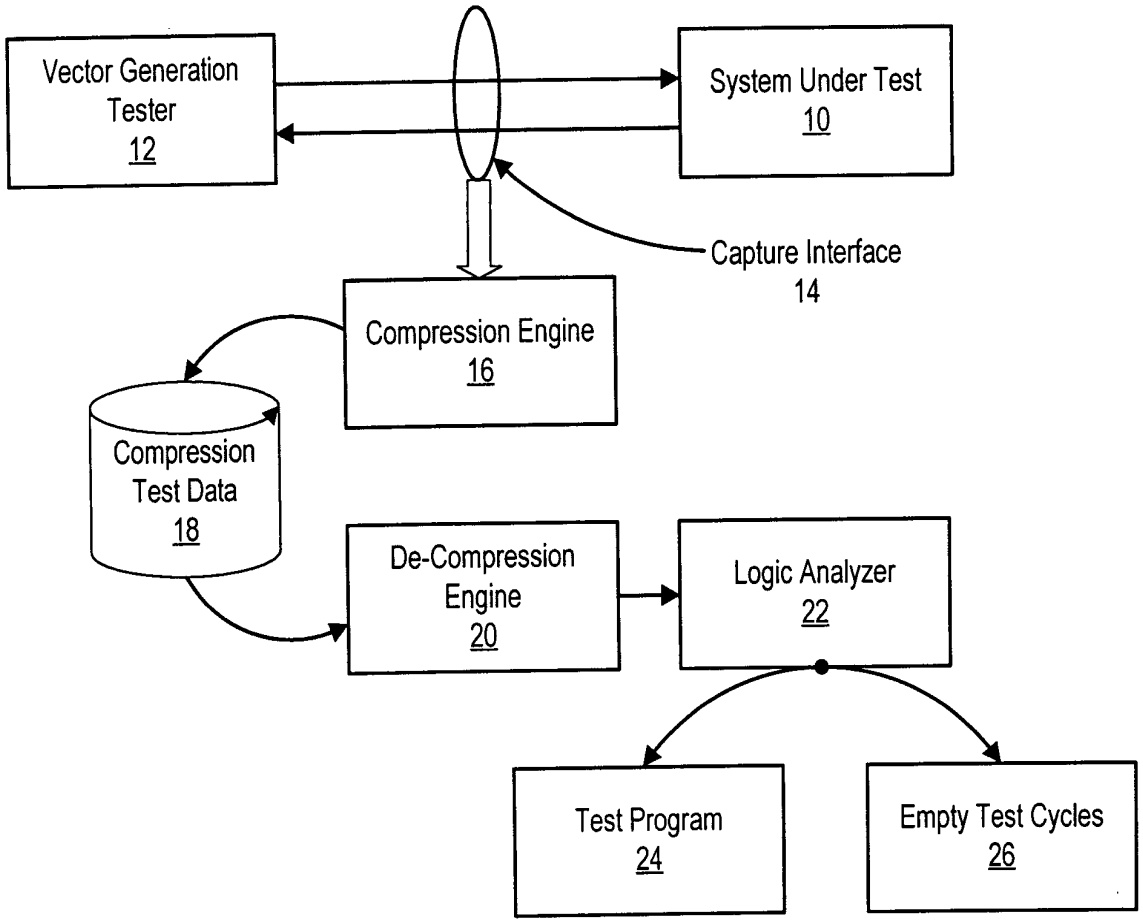
Vector Generation
Tester
12
System Under Test
10
Capture Interface
14
Compression Engine
16
Compression
Test Data
18
De-Compression
Engine
20
Logic Analyzer
22
Test Program
24
Empty Test Cycles
26

Figure 1

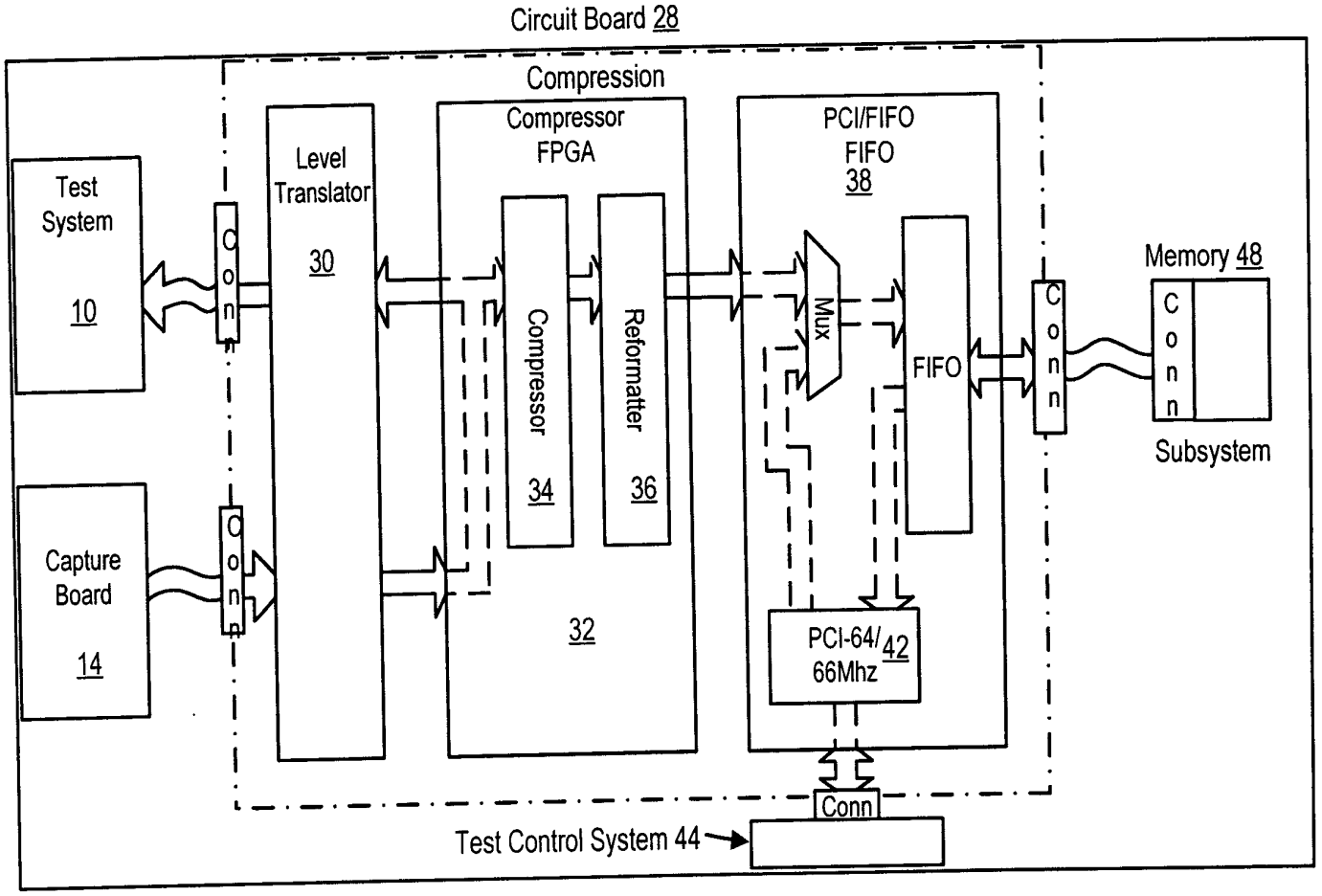
Circuit Board 28
Compression
Compressor FPGA
PCI/FIFO FIFO 38
Level Translator 30
Test System 10
Capture Board 14
Conn
Conn
Compressor 34
Reformatter 36
32
Mux
FIFO
Conn
Memory 48
Conn
Subsystem
PCI-64/66Mhz 42
Conn
Test Control System 44

Figure 2

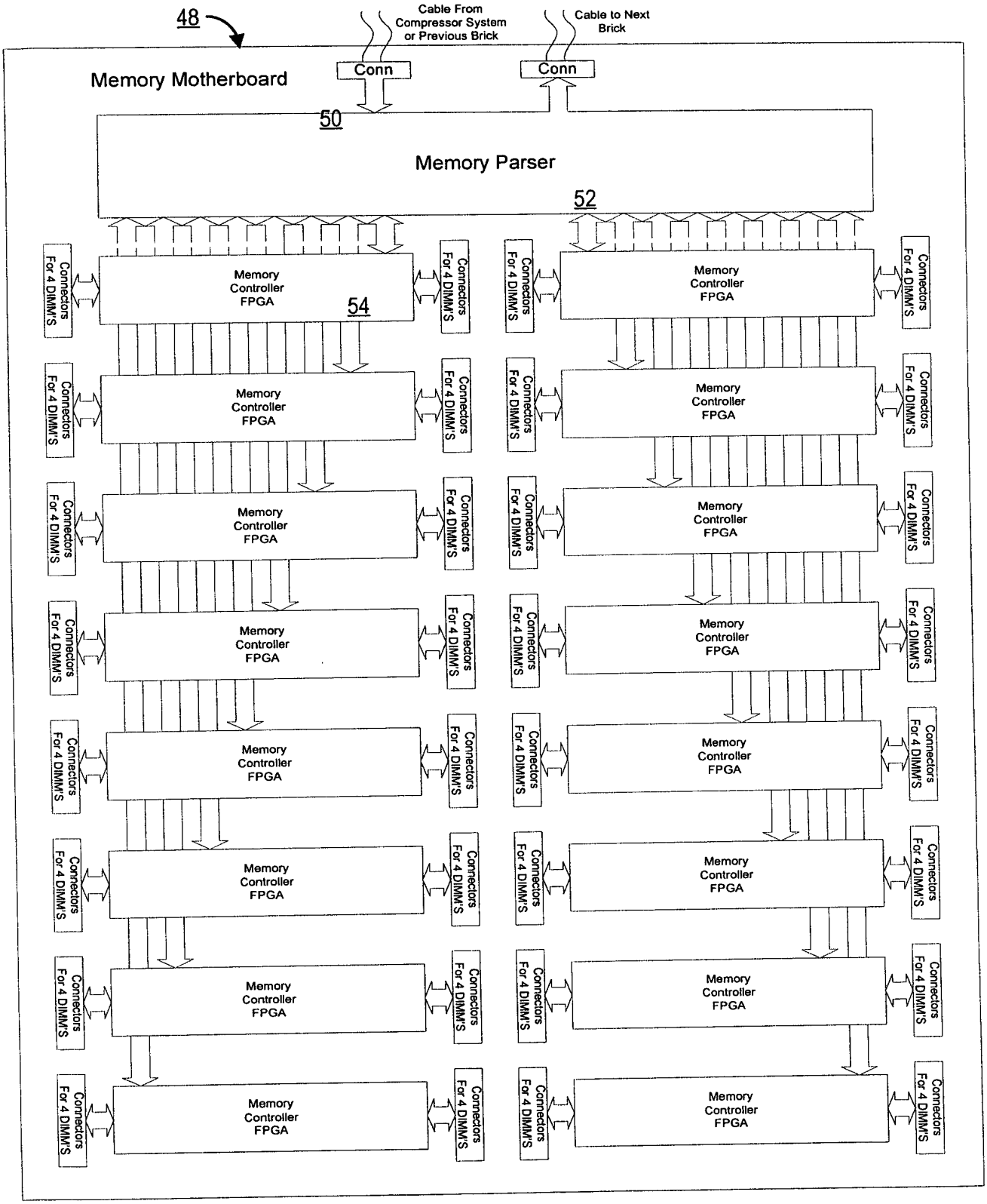
48
Cable From Compressor System or Previous Brick
Cable to Next Brick
Memory Motherboard
Conn
Conn
50
Memory Parser
52
Memory Controller FPGA
54
Connectors For 4 DIMM'S

Figure 3

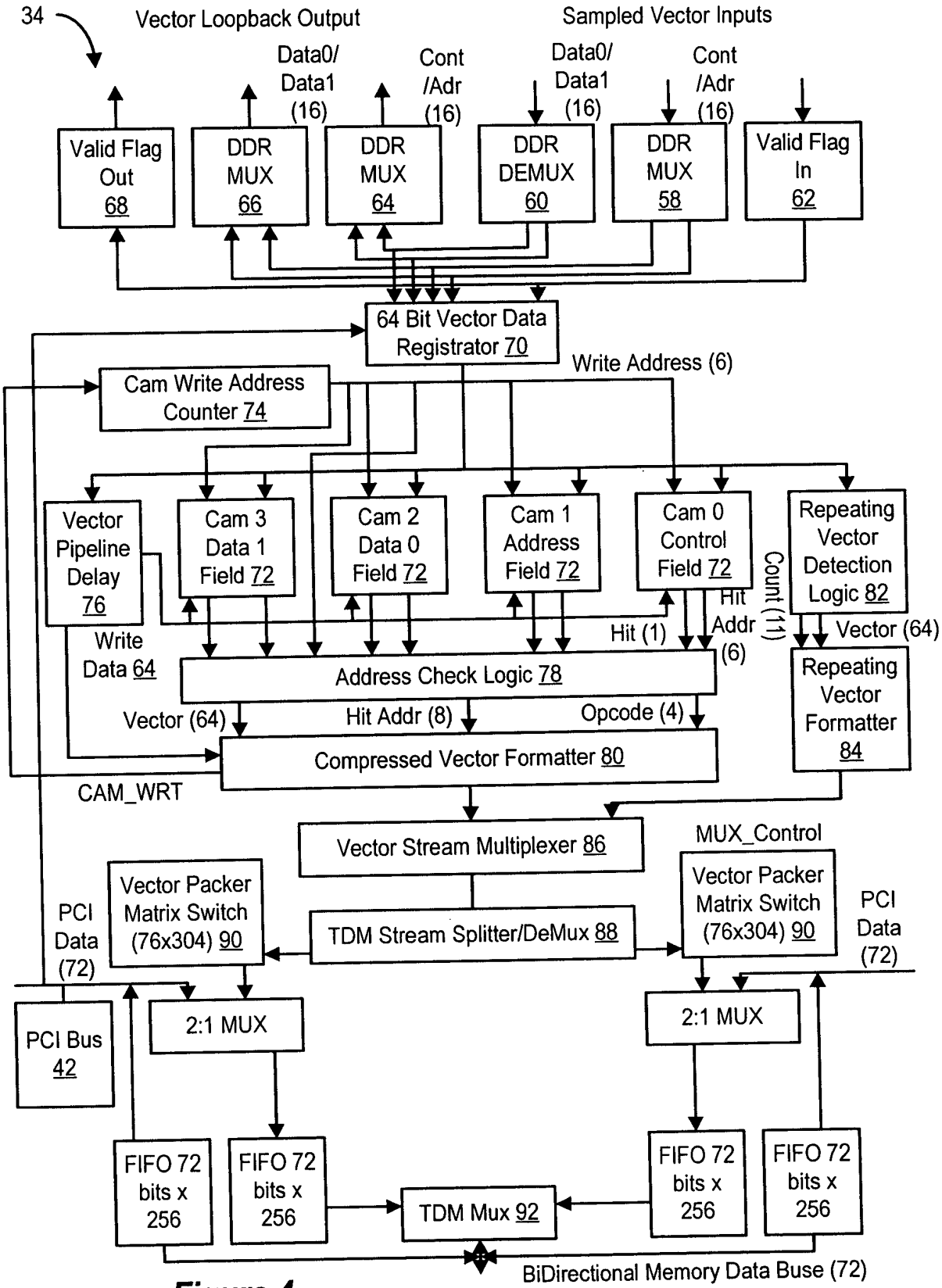
34
Vector Loopback Output
Sampled Vector Inputs
Data0/ Data1 (16)
Cont /Adr (16)
Data0/ Data1 (16)
Cont /Adr (16)
Valid Flag Out 68
DDR MUX 66
DDR MUX 64
DDR DEMUX 60
DDR MUX 58
Valid Flag In 62
64 Bit Vector Data Registrator 70
Write Address (6)
Cam Write Address Counter 74
Vector Pipeline Delay 76
Cam 3 Data 1 Field 72
Cam 2 Data 0 Field 72
Cam 1 Address Field 72
Cam 0 Control Field 72
Repeating Vector Detection Logic 82
Count (11)
Hit Addr (6)
Hit (1)
Vector (64)
Write Data 64
Address Check Logic 78
Repeating Vector Formatter 84
Vector (64)
Hit Addr (8)
Opcode (4)
Compressed Vector Formatter 80
CAM_WRT
Vector Stream Multiplexer 86
MUX_Control
Vector Packer Matrix Switch (76x304) 90
TDM Stream Splitter/DeMux 88
Vector Packer Matrix Switch (76x304) 90
PCI Data (72)
PCI Data (72)
PCI Bus 42
2:1 MUX
2:1 MUX
FIFO 72 bits x 256
FIFO 72 bits x 256
TDM Mux 92
FIFO 72 bits x 256
FIFO 72 bits x 256
BiDirectional Memory Data Buse (72)

Figure 4

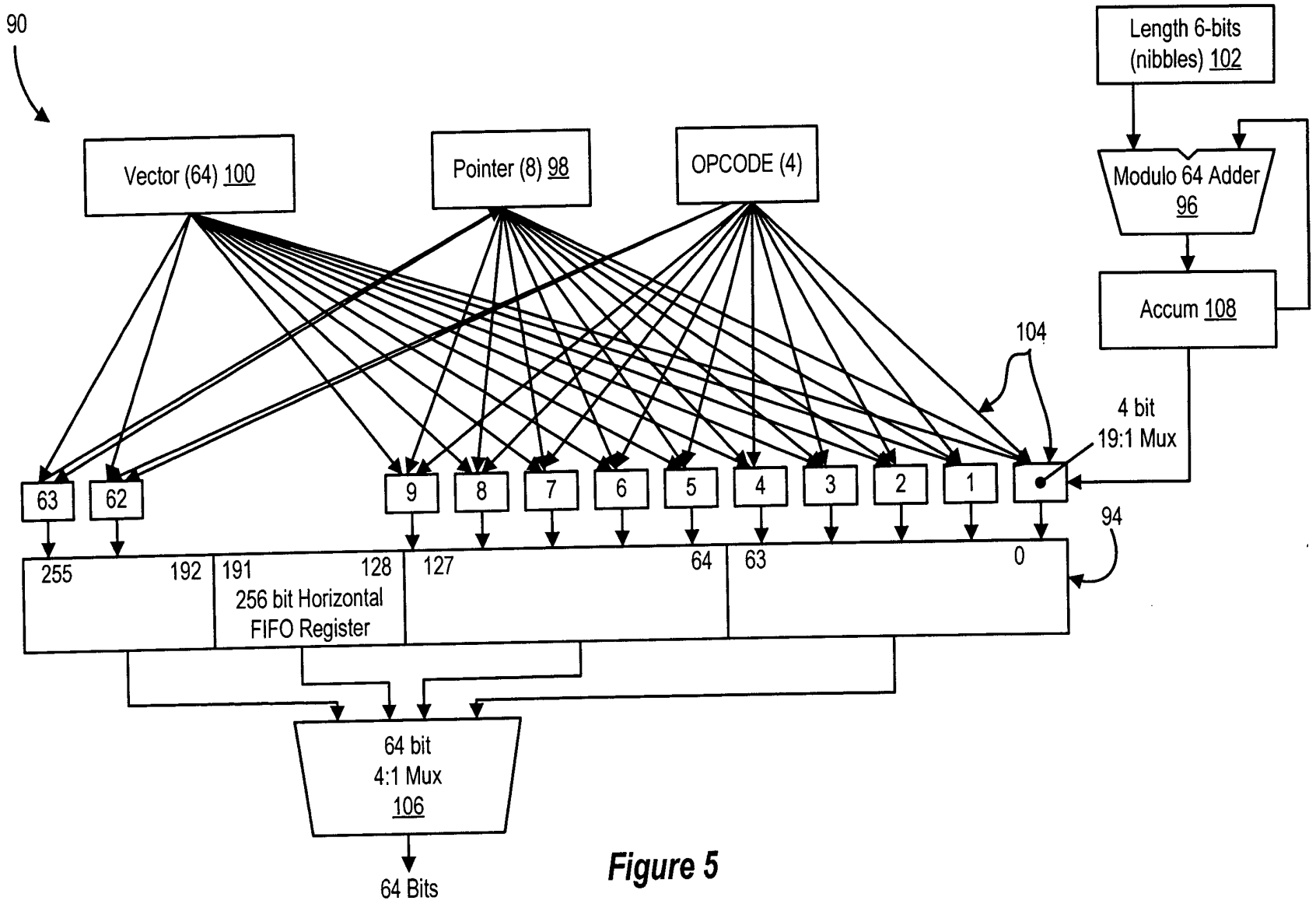
90
Length 6-bits
(nibbles) 102
Vector (64) 100
Pointer (8) 98
OPCODE (4)
Modulo 64 Adder
96
Accum 108
104
4 bit
19:1 Mux
63
62
9
8
7
6
5
4
3
2
1
94
255
192
191
128
127
64
63
0
256 bit Horizontal
FIFO Register
64 bit
4:1 Mux
106
64 Bits

Figure 5

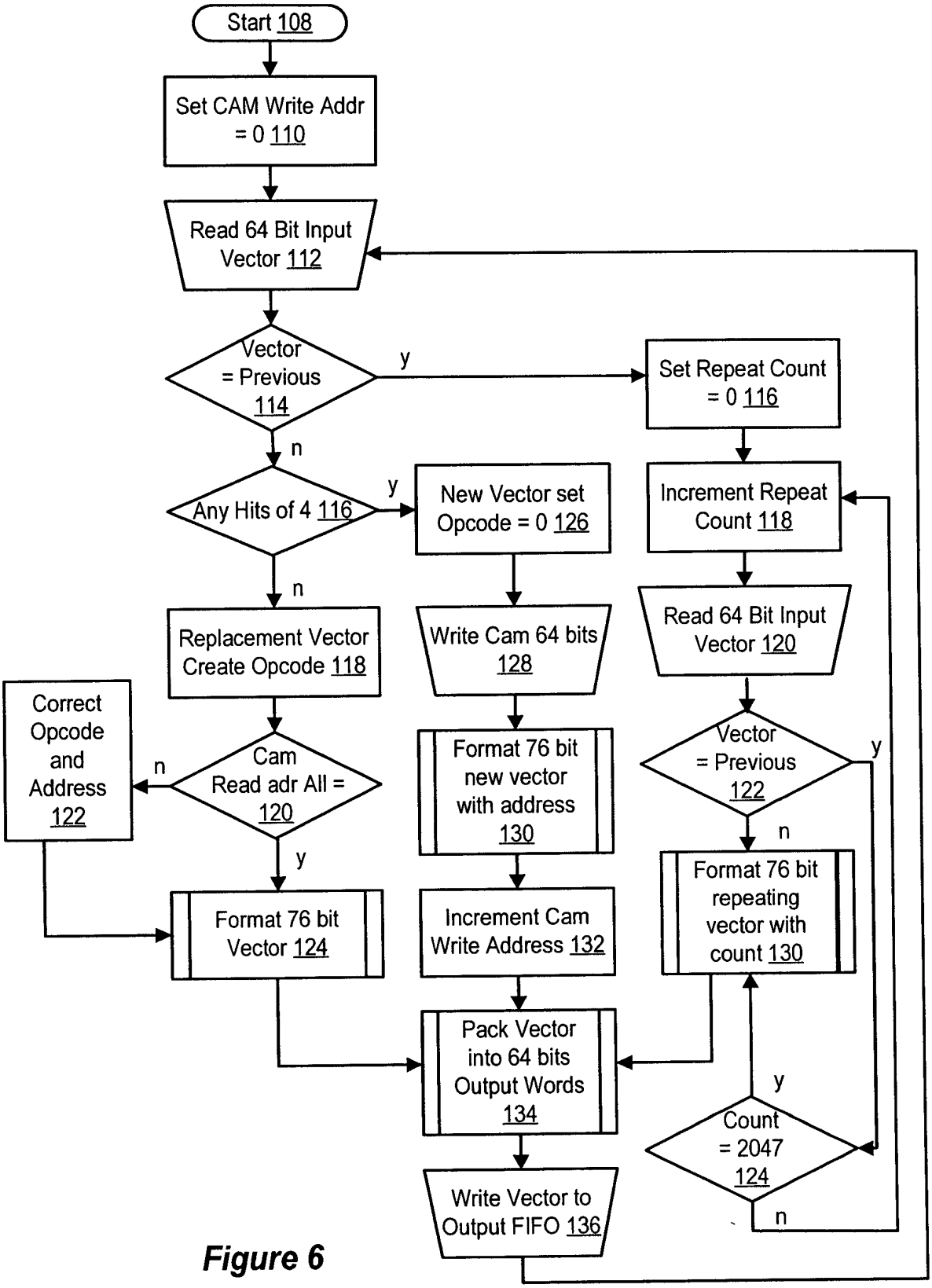
Start 108
Set CAM Write Addr = 0 110
Read 64 Bit Input Vector 112
Vector = Previous 114
y
Set Repeat Count = 0 116
n
Any Hits of 4 116
y
New Vector set Opcode = 0 126
Increment Repeat Count 118
n
Replacement Vector Create Opcode 118
Write Cam 64 bits 128
Read 64 Bit Input Vector 120
Correct Opcode and Address 122
n
Cam Read adr All = 120
Format 76 bit new vector with address 130
Vector = Previous 122
y
n
y
Format 76 bit Vector 124
Increment Cam Write Address 132
Format 76 bit repeating vector with count 130
Pack Vector into 64 bits Output Words 134
y
Count = 2047 124
Write Vector to Output FIFO 136
n

Figure 6

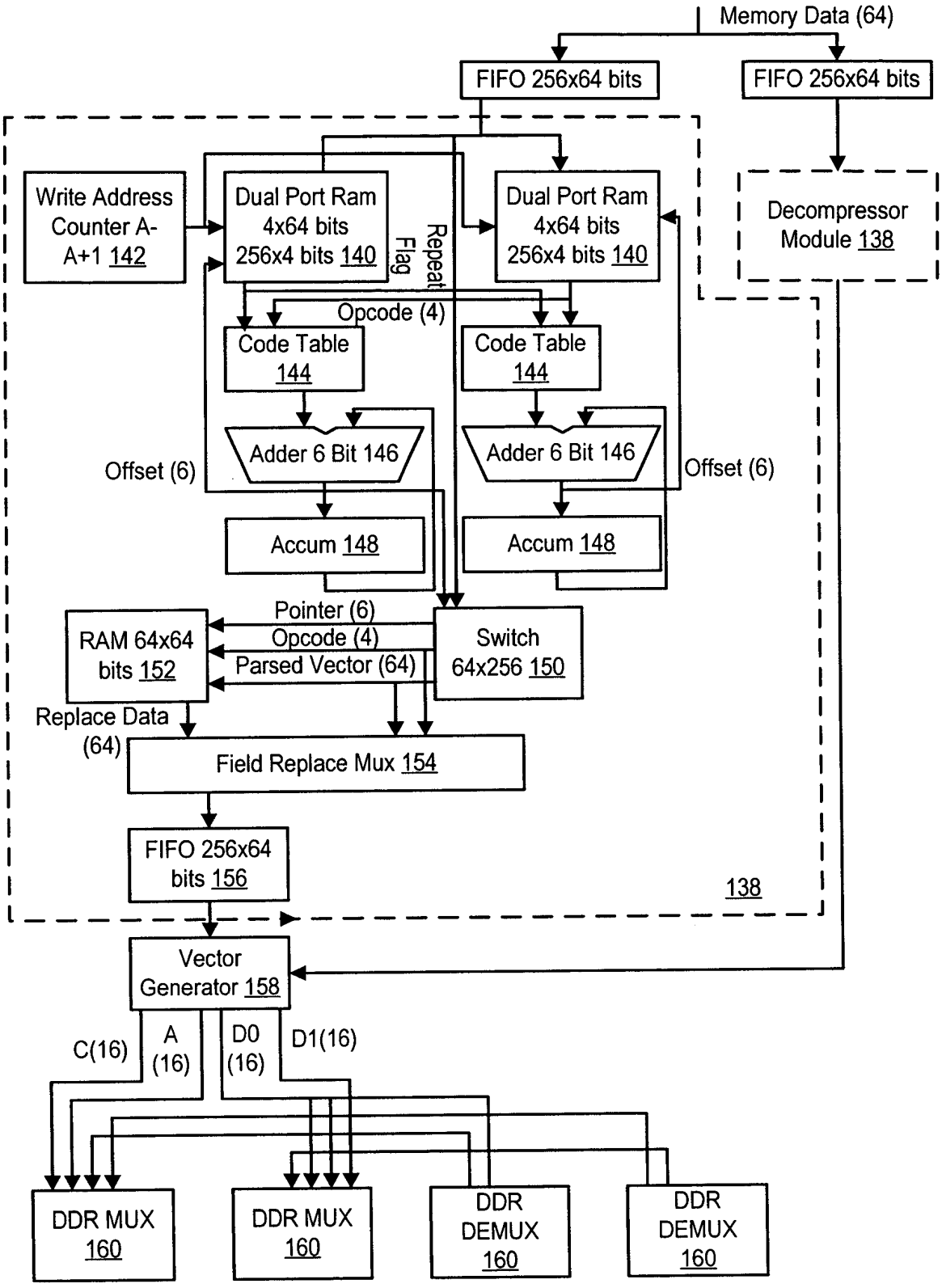
Memory Data (64)
FIFO 256x64 bits
FIFO 256x64 bits
Write Address Counter A-A+1 142
Dual Port Ram 4x64 bits 256x4 bits 140
Repeat Flag
Dual Port Ram 4x64 bits 256x4 bits 140
Decompressor Module 138
Opcode (4)
Code Table 144
Code Table 144
Adder 6 Bit 146
Adder 6 Bit 146
Offset (6)
Offset (6)
Accum 148
Accum 148
Pointer (6)
Opcode (4)
Parsed Vector (64)
RAM 64x64 bits 152
Switch 64x256 150
Replace Data (64)
Field Replace Mux 154
FIFO 256x64 bits 156
138
Vector Generator 158
C(16)
A (16)
D0 (16)
D1(16)
DDR MUX 160
DDR MUX 160
DDR DEMUX 160
DDR DEMUX 160

Figure 7